Integrated circuit design for reduced EMI

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Radiation of electromagnetic interference is a problematic side-effect of digital electronic systems. Radiation becomes amplified as it conducts and radiates from an integrated circuit to a PCB and beyond the system. While proficient system level design is paramount, the design of the ICs can help to control EMI by minimizing the source of the radiation. Aspects of IC design that can be optimized in order to minimize the levels of radiation are described in this paper which was first presented at the EMC '99 Zurich Symposium.

In electronic designs, radiated electromagnetic emissions are caused inadvertently by current and voltage transients which result from high-frequency switching, and fast rise or fall times of digital logic. The transients are either conducted or coupled onto the power lines, signals, and other components throughout an electronic system. The printed circuit board (PCB) provides the antennas from which most of the radiation is broadcast, and the characteristics of the digital logic produce the emissions that are broadcast by the PCB.

The selection of components for a PCB determines the amount of 'source capability' for radiation, and the placement and routing of the components and signals determine the 'radiation efficiency' of the PCB. Since the major sources of emissions are VLSI circuits, many designers who engineer PCBs are actively searching for ICs with low radiated emissions characteristics. Figure 1 illustrates the interaction of ICs and PCBs, and the subsequent emissions which radiate from the components of the system. This paper summarizes todays best known practices that can be applied to improve the EMI performance of new processor designs.

EMI creation from CMOS transient current

A major source of high-frequency harmonic radiation is the peak of current which is created by each logic transition. The harmonic content and the amplitude of the current depends upon the switching characteristics of the transistors and the wave shape of the signals that they produce.

In CMOS technology, two phenomena contribute to this current. One contributor is the through-current of the gates (also called 'crowbar current' or 'shoot-through current'), resulting from the overlapping of the rise and fall times of the P and N channel output transistors. This is illustrated as current I_x in figure 2.

The second EMI contributor is the current delivered by the gate to the output load capacitance referenced to the ground or to the V_{ss}. This capacitance is the sum of the parasitic substrate capacitance, the parasitic capacitance of the following gate, and the external connections in case of external I/O buffer.

As this capacitor is referenced to ground or V_{ss}, the current through the power supply flows only on rising transitions, as illustrated by IC current in figure 2. During the falling edge output transition, the current from the capacitance is dissipated through the N channel transistor and the substrate resistance.

Figure 1: System-level electromagnetic radiation

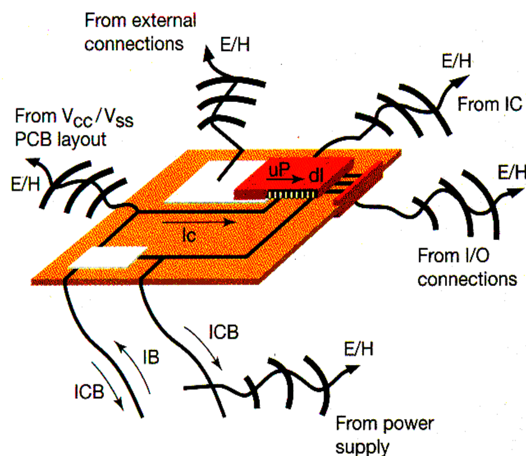
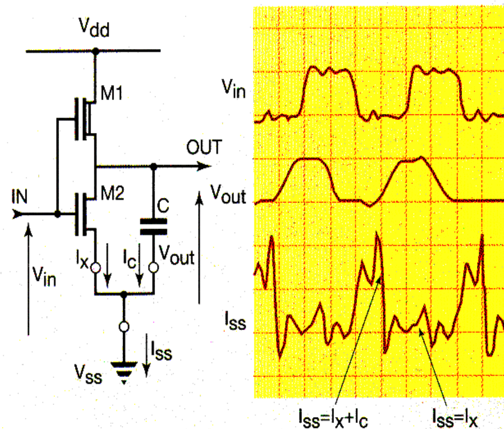


Figure 2: Switching current wave form



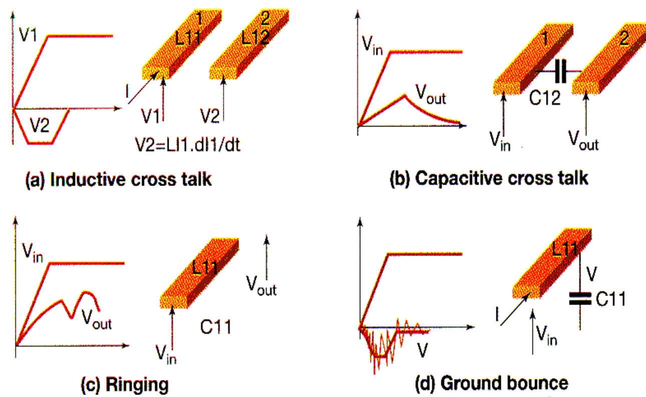


Figure 3: Distributed lead inductance and capacitance

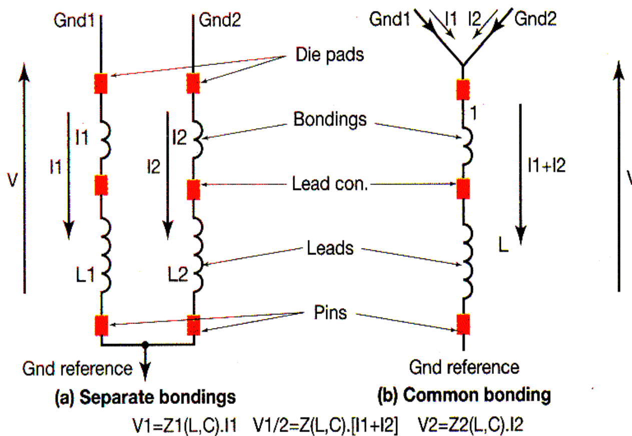


Figure 4: Noise coupling with common bonding

Several aspects of a typical IC design flow influence the electromagnetic characteristics of the IC. From the macro-level package design to the micro-level logic cell design, EMI can be minimized or maximized at almost every step of the process.

At high clock frequencies, for currents that result from internal signal transitions in CMOS integrated circuits, a perfect conductor does not exist. Propagation rate and amplitude are limited, and both depend on the relative resistivity of the conductors.

Furthermore the parasitic distributed capacitance and inductance oppose a change in any voltage or current. This is not only true for external connections on the PCB, but also for the internal lead frame connections. As the phenomena are proportional to the size of conductors through which the current flows, the choice of the package model, in the case of a sensitive application, becomes very important for EMI performance. If the designer is not free to select the package that will provide the best EMI performance, he has to optimize the die pad connection locations versus the lead frame, taking into account all the parasitic elements of the package which has been selected.

Parasitic inductance and capacitance of the bond wires and of the lead connections are the major distributors of chip-level high frequency noise radiation. Inductance and capacitance between leads creates cross talk between the different signal that can help to carry out of the device high internal clock frequencies and harmonics.

Ground inductance and capacitance reduce the time rate of the signal propagation and generate spurious resonant frequency responsible for high frequency ringing or ground noise.

Package size

The parasitic effects in IC packages depend on the mechanical dimensions of the lead frame. Consequently, the electromagnetic noise which is radiated by a device is highly dependent on the type of package which is used for device assembly. Long leads that are close together generate undesirable high levels of mutual inductance and capacitance.

To reduce EMI, the package and leadframe must be selected with the shortest leads possible, and with the leads not congested together. The final selection can be made based on the most critical dimensions. Generally, small package sizes give better results, but care should be taken to avoid cross-talk phenomena of key signals which can create high frequency noise. Table 1 shows an example of lead inductance variation versus package type.

Separate bonding, separate ground connections

In CMOS technology, ground reference voltage and return ground current paths are in most cases very sensitive to signal integrity or high frequency noise. All of the transistors are referenced on the substrate, and internal gates loads are directly connected to the substrate. Parasitic elements of the package prevent achieving a good voltage reference.

At high clock frequencies, the most important parameter is the inductance of the

Table 1: Typical lead inductances for various package types

Package model	68-pin PLCC	28-pin PLCC	132-pin PQFP
Middle pin inductance	10.5nH	5.3nH	12.2nH
Corner pin inductance	23nH	7nH	18.1nH

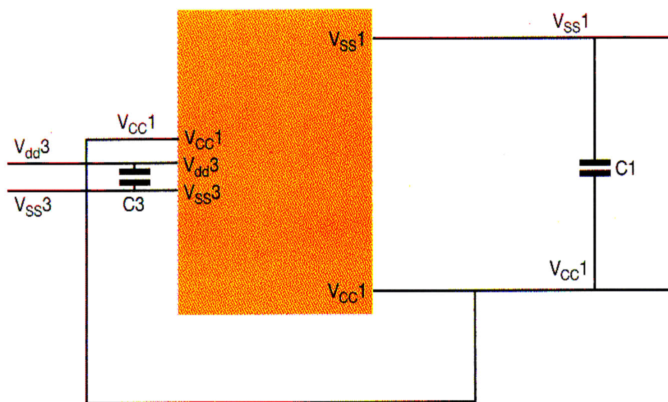


Figure 5: Typical case of bad and good pin assignment

connection. Depending on the package size, the inductance of the bonding wire is in the range of 1nH to 3nH, and the inductance of the lead can vary from 5nH up to 40nH. Connecting onto the same die pad two separate power supplies introduces spike problems affected by L.di/dt issues.

Due to this spurious inductive coupling between two modules, serious signal integrity problems may develop, but also it can cause EMI problems due to signal lines modulated by high clock harmonic frequencies or high frequency ground bounce resulting from the LC characteristic of the bonding and lead connection.

Pin assignments

On a PCB, the power distribution is provided by supply and return traces connected to dedicated pins of the components. The impedance of these connections and the length of the PCB traces (generally inductive) are not important if the signal frequency is low, but rapidly become critical when the frequency increases. This is particularly true for digital signals which, due to the high switching speed, contain high frequency harmonics. To avoid excessive high frequency voltage drop, a ceramic capacitor is generally connected to the supply pins of the IC. It provides the inrush current that logic gates need to switch properly, and it avoids high frequency current flowing through the power PCB traces .

Maxwell's equations predict that the radiated electromagnetic field strength produced by the switching currents increases with the amplitude of the current, with the frequency of the signal, and also with the length and area of connections on the chip as well on the PCB. The resulting radiation comes from anywhere high frequency currents are flowing on the die, on the filtering loop and components, and even through the connections to the battery.

Any loop of current created by the power lines, by the clock distribution or the I/O connections or the external components constitutes an important source of electromagnetic disturbance. The amount of radiated energy is proportional to the total loop area. For reducing EMI, it is very important to optimize the pin locations on the device. Position of critical pins must be chosen to provide the shortest connections possible on the chip as well as on the PCB.

V_{dd}/V_{ss} for core logic

To preserve the signal integrity and to minimize the electromagnetic disturbance, it is good practice to separately power the logic module that is particularly noisy, from the other functions of the circuit, like digital I/O or analogue circuits.

In most of the design, the on-chip digital logic, called processor core or nucleus, should be isolated from the peripheral part that contains all the interface logic (i.e. I/O) of the integrated circuit.

The power V_{ddl} and ground pins V_{ssl} of the core logic should be placed close together. This makes it easier for the PCB designer to place the filtering capacitor close to the power and ground pins on the PCB. Consequently the power impedance is kept low, with a small inductive component, and the V_{ddl} voltage drops which result from the high frequency variation of currents are confined to within the chip nucleus, where no significant antenna effect exists.

Due to high frequency peaks of current generated by the logic core, the location of the pins must be selected so that the connections have the minimum inductance in order to avoid ringing. This can be achieved by using pin locations in the middle of the package side, because the lengths of the bonding wires and the lead frame are shorter in the middle than in the package corners.

Separately powering the core part of the circuit and the input/output part of the circuit helps to isolate the high frequency noise generated by the core logic from radiating through the I/O control circuits. When the I/O and core logic have the same power supply, the noise from the core logic is conducted onto the I/Os and is radiated through I/O connections throughout the application.

Figure 5 represents practical pin assignments. It shows on the same product two cases of selection: one bad and a correct assignment. The powering of the logic part is incorrect because the power pins and the ground pin have been placed at two different and opposite corners. Furthermore, another powering pin is located at opposite side of the package. However, the powering of the analogue part (V_{dd3}/V_{ss3}) is correctly placed in the middle of the die side, and the two pins are located close together.

Clock oscillator

The clock oscillator is often considered as the most important source of radiated electromagnetic energy. This is mainly because the crystal drive current needs to be large in order to compensate the energy loss in the crystal; otherwise, oscillation does not start. The equivalent loop created by the crystal, the external components and the PCB traces correspond to a radiating area that is large when compared to the die size itself.

Furthermore, the crystal acts as a real impedance not only at resonant frequency but also at all the harmonics of the fundamental frequency, so the output signal is a quasi square signal. Such a signal generates high frequency radiation, and high frequency conducting currents through the power supply of the clock module and through the other power supplies if any are connected. For all of these reasons, the clock oscillator must be carefully isolated and powered separately.

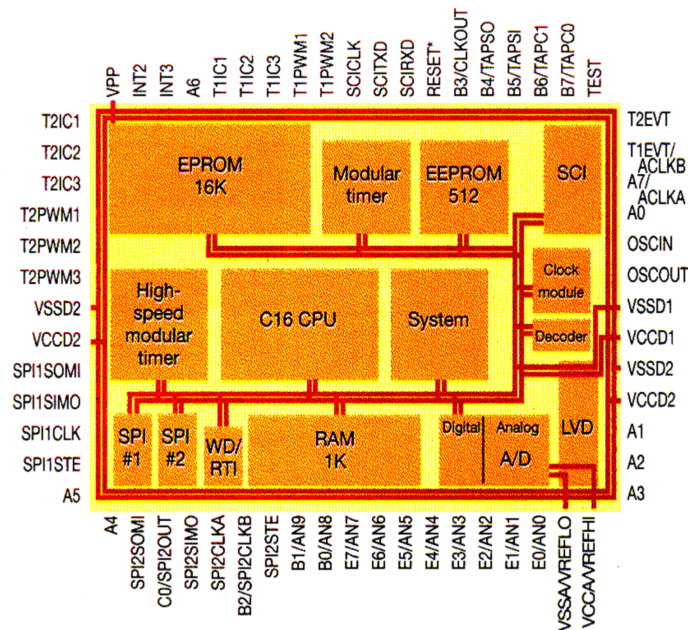


Figure 6: Separate power rails for core and I/Os

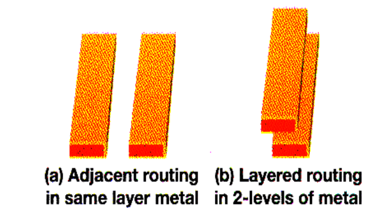


Figure 7: Adjacent and layered routing

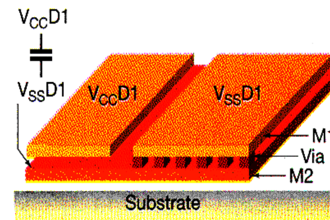


Figure 8: On-chip distributed power-to-ground capacitance

To minimize as much as possible the inductive effect of the connections, the oscillator should be placed not in a corner of the package but at the middle side edge of the package. The oscillator input and output pins must be placed so that the disturbance loop can be reduced as much as possible. There should be no sensitive inputs near the oscillator pins. The oscillator input and output pins should be located between the oscillator's power pin V_{ddc} and return current V_{ssc} pin. This provides some shielding and also allows for short PCB connections.

I/O and control

With the CMOS process, the output buffers are generally important sources of noise. The reason is that the peaks of current (sometimes 100mA or more) flow at each clock edge.

A part of this current is due to the overlapping of conduction times of the N and P channel transistors, and the other component comes from the current that flows through the capacitance at the output of the buffer. The largest amplitude is reached during the switching transition from low to high when the output loads the external capacitor through the pins and package inductance.

This is the reason why the fast buffers should be connected to the middle package edge where the leads are shortest and closest to the related ground to reduce the transmission line impedance on the PCB. This is not as critical in case of slow transition buffers.

Isolation of noisy logic from I/Os and sensitive circuitry is crucial toward minimizing radiated emission from a VLSI design. Likewise, the power rails for digital logic should not be connected to the power rails for I/Os. The I/Os should have V_{dd}/V_{ss} routes that are separate from those of the core digital logic. This methodology will help to keep the high-frequency energy generated within the core from being transmitted over the I/O package lead frame and across the PCB routing. Figure 6 illustrates power isolation of core digital, frame I/O, and analogue circuitry.

Core logic V_{dd} is better either adjacent to or layered with core logic V_{ss}. Layered routes provide the most V_{dd}-to-V_{ss} routing capacitance as well as the minimum radiating loop area for the transients that ride on these power rails.

However, if only two metal layers are available, then adjacent routing may be necessary in order to allow for routing signals from one side of the power rails to the other side. Figure 7 illustrates adjacent and layered routing. Adding on-chip distributed capacitance by routing V_{ss} over or under V_{cc} whenever space is available can also help to reduce RE and improve the noise margins of the digital logic. Figure 8 illustrates distributed power-to-ground capacitance. Running V_{dd}/V_{ss} rails adjacent to I/O V_{dd}/V_{ss} rails for long distances should be avoided. When necessary, cross I/O V_{dd}/V_{ss} rails only at 90° angles. All of these precautions are intended to minimize coupling of core noise onto I/O pins.

Module placement

The location of each module, relative to the power supply pins, also influences the emissions of digital modules.

- Clock module: The clock module should be located near the middle of one side of the device, and the signals should have the shortest routes available to the bond-pads.
- CPU, system, decoder, EEPROM, RAM: These modules basically can be placed anywhere. These modules should be located in a manner that minimizes routing of address, data, and system clock signals.
- Timer, SPI, SCI, other digital peripheral modules: These modules can be located wherever space allows. However, it is good practice to locate the modules with higher frequency switching closer to digital power supply pins.

Importance for low EMI

It is very common for the oscillator to generate the highest levels of emissions from

an IC. Consequently, it is very important to optimize the chip design in the area of the oscillator.

The CMOS gate-oscillator design is often responsible for the high emissions content of the oscillator. Gate-oscillators usually provide rail-to-rail switching at frequencies in the megahertz or tens-of-megahertz ranges. This is a bad combination for EMI. Moreover, the oscillator has an external radiating loop. While EMI-generating system clock currents are contained within very small circuits inside of the IC, the oscillator currents extend outside of the IC package, conducting through the package lead frame, and then flow through PCB traces, external capacitors, and a resonator.

PLL oscillators have several advantages over /2 and /4 oscillators for reducing emissions. The most significant effect is that the external reference crystal operates at a slower frequency in PLL designs than in standard oscillator configurations.

Reducing the oscillator frequency serves to move the entire emissions spectrum toward lower frequencies, and thus to reduce the emission levels at higher frequencies, which include the communication bands. Figure 9 illustrates how harmonics of lower-frequency oscillators fall off faster than those of faster oscillators.

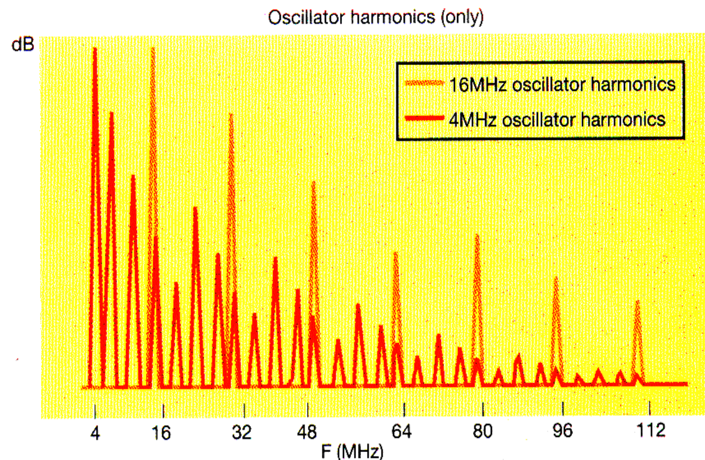


Figure 9: Theoretical trailing off of harmonics

Spread-spectrum effect

Some PLLs produce a frequency dithering effect which serves to 'spread the spectrum' of internal system clocks. The spread spectrum effect helps to reduce the amplitude of emissions spikes by widening the profile of the spike. The same amount of energy is still present, but it becomes dispersed over a slightly larger span.

For low EMI, static is much better than dynamic architecture design. Since every logic cell of a dynamic architecture is updated on every clock cycle, the simultaneously switching transient currents are relatively high with this type of architecture.

However, since static logic requires an update only when its logic state changes, the number of cells switching simultaneously is significantly lower with a static design. Less transient current translates directly into less EMI. Since EMI is relative to the amplitude of switching voltage, reducing the V_{dd} power rail also provides a reduction of EMI.

While it is important to design all clock drivers with enough strength to drive their loads, it is also important not to over-design - to make the drivers excessively large. A driver that switches faster or harder than required creates unnecessary RE.

Since RE is proportional to the number of logic cells that are changed or updated, disabling clock trees to unused modules or signals can help to reduce RE. For example, if a device has an SPI module that it only uses half of the time, then turning off the clocks to that module during its 'idle'-time will help to reduce the overall RE from the device.

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