Signal Integrity issues and circuit interconnect characterization.

Circuit Signal Integrity (SI) issues are:

- Reflections,
- Crosstalk,
- Propagation delay,
- Loss,
- Groundbounce,
- Dispersion.

Consequences of poor SI, i.e. crosstalk, reflections and ringing are:

- signal distortion and digital switching errors giving low functional performance,
- impact on wider EMC issues,
- increased costs from design failure and application problems/recalls,
- delays in time critical projects.

To prevent these problems it is necessary to perform and verify Spice and Ibis based simulations at IC and PCB level with accurate interconnect models.

At high speeds interconnects become transmission lines and discontinuities become lumped L – C elements. Time Domain Reflectometry (TDR) and Vector Network Analysis (VNA) may be utilized for circuit interconnect characterization, by applying an "Inverse Scattering" technique. This is where an ideal model is created to approximate to the DUT measurements and is used to produce simulated parameters for comparison with measured values.

A comparison of the two measurement techniques is useful.

Principles of Vector Network Analysis (VNA):

This is a frequency domain measurement utilizing the amplitude and phase characteristics of reflected and transmitted sine waves applied to the DUT.

Principles of Time Domain Reflectometry (TDR):

This is a time domain measurement using a fast rising edge stimulus that is applied to the DUT. The reflected waveform signature may be analysed to determine distributed circuit parameters.

There are certain advantages of Time Domain Reflectometry compared to Vector Network Analysis for SI characterisation:

- A step stimulus technique is better suited to the analysis of wideband digital circuits.
- Capability for definition of isolated circuit portions, rather than creation of single element or behavior model, i.e. time domain measurement and model correlates to the physical DUT geometry.
- Easy determination of effective dielectric constant from trace length & time delay.
- Inherent differential analysis.
- Simpler normalization procedure.

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