Groundbounce associated with package and PCB.

PSpice simulation to explore indirect common-mode effects from IC internal load-charging transient currents.

A series of 5 circuits Figures 1 to 5 and associated plots Plots 1 to 5.

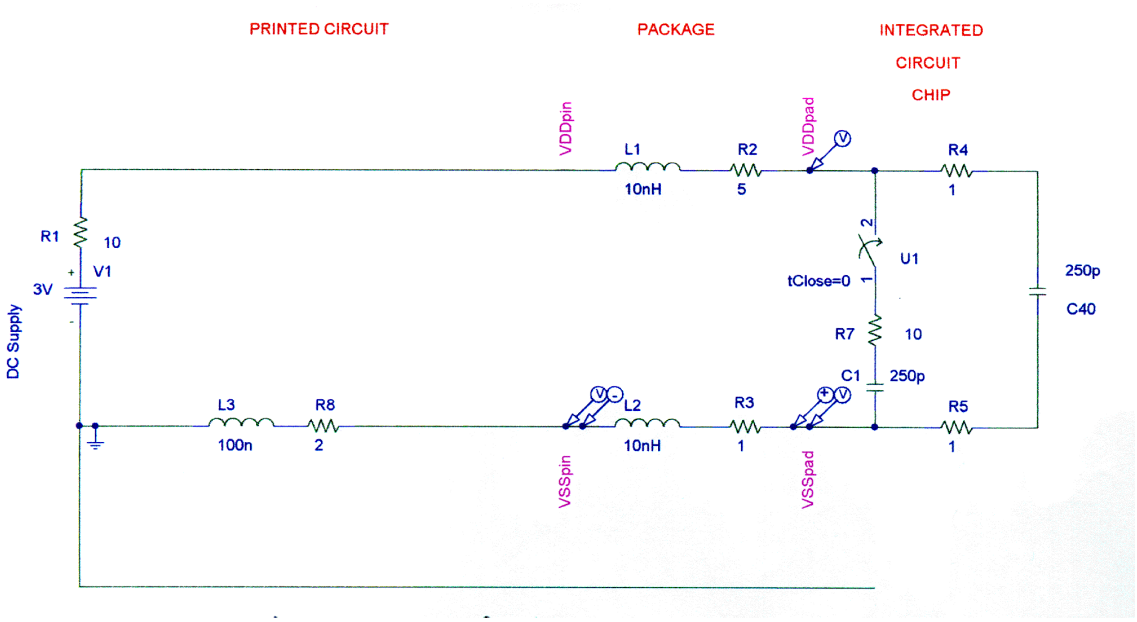


Figure 1. Initial. This is a simplified model of a circuit that is in three parts:

Digital IC silicon chip; consisting of simplified digital core, where U1 is an instantaneously closed switch, C1 is the sum of parasitic substrate capacitance plus capacitance of following gates and C40 is some on-chip decoupling/bypassing capacitance.

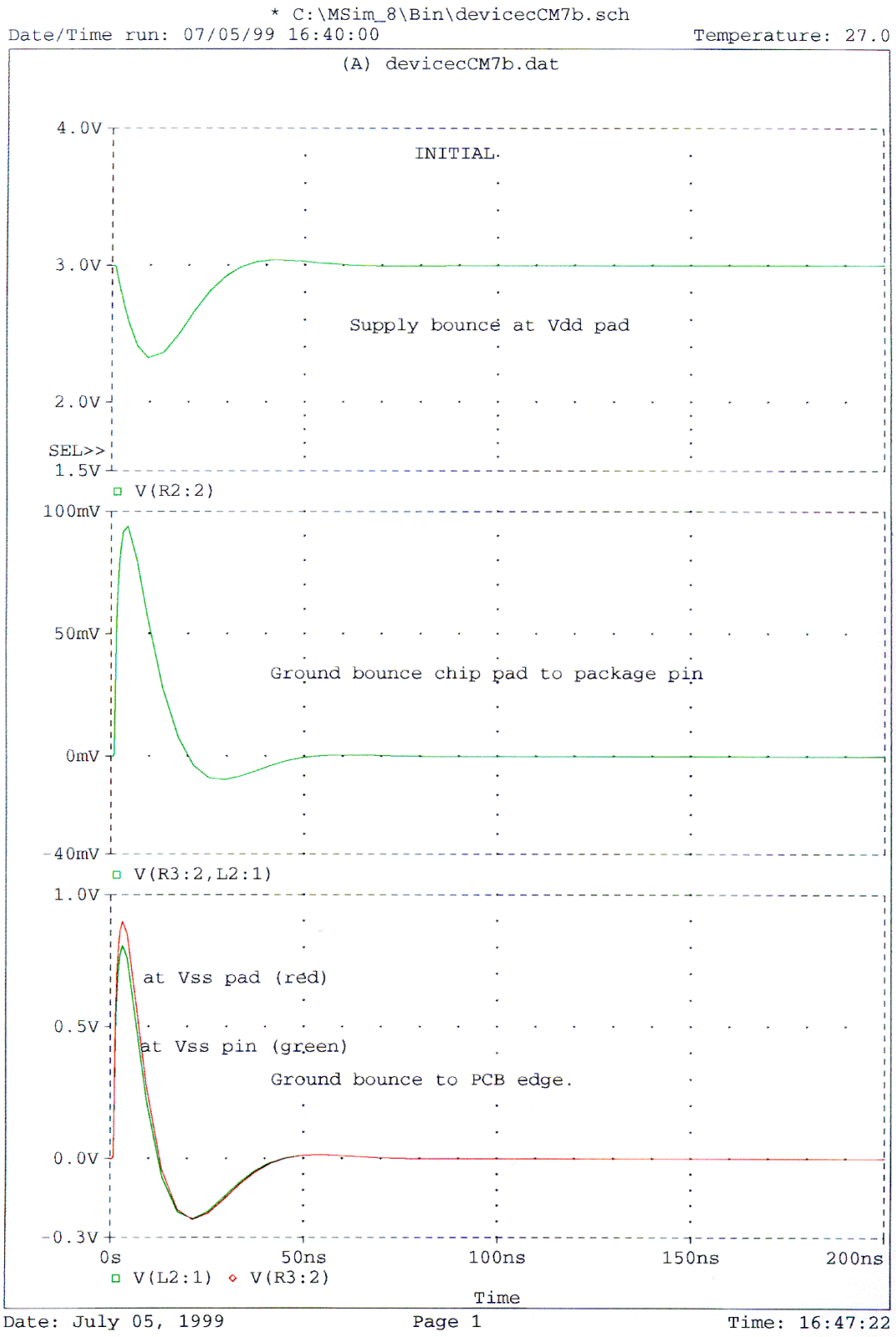
Package; with bondwire and leadframe inductance and resistance. (Plus some damping resistance incorporated in R2).

The PCB circuit; with DC supply and L3 ground inductance.

Plot 1, (over)

When the switch is closed the transient voltage “bounce” at three points is recorded:
a) (top plot) chip Vdd supply pad to PCB ground,
b) (middle plot) across Vss chip pad to Vss pin,
c) (bottom plot) chip Vss ground pad to edge of PCB ground.

Notice there is almost 1V. of ground bounce across Vss pin to edge of board.



Plot 1a (top), Plot 1b (middle), Plot 1c (bottom).

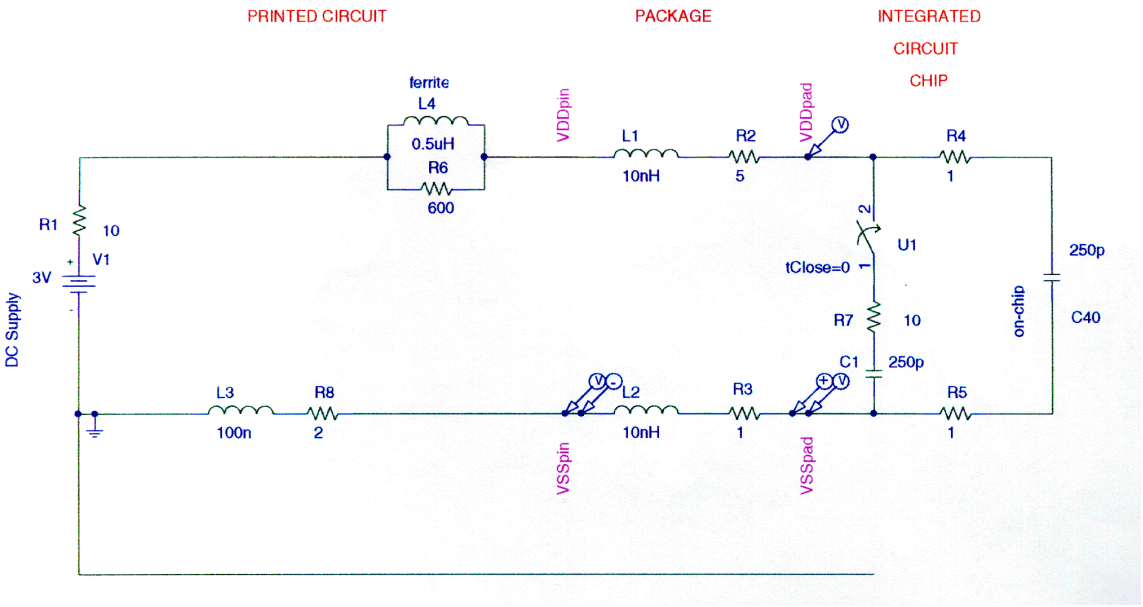
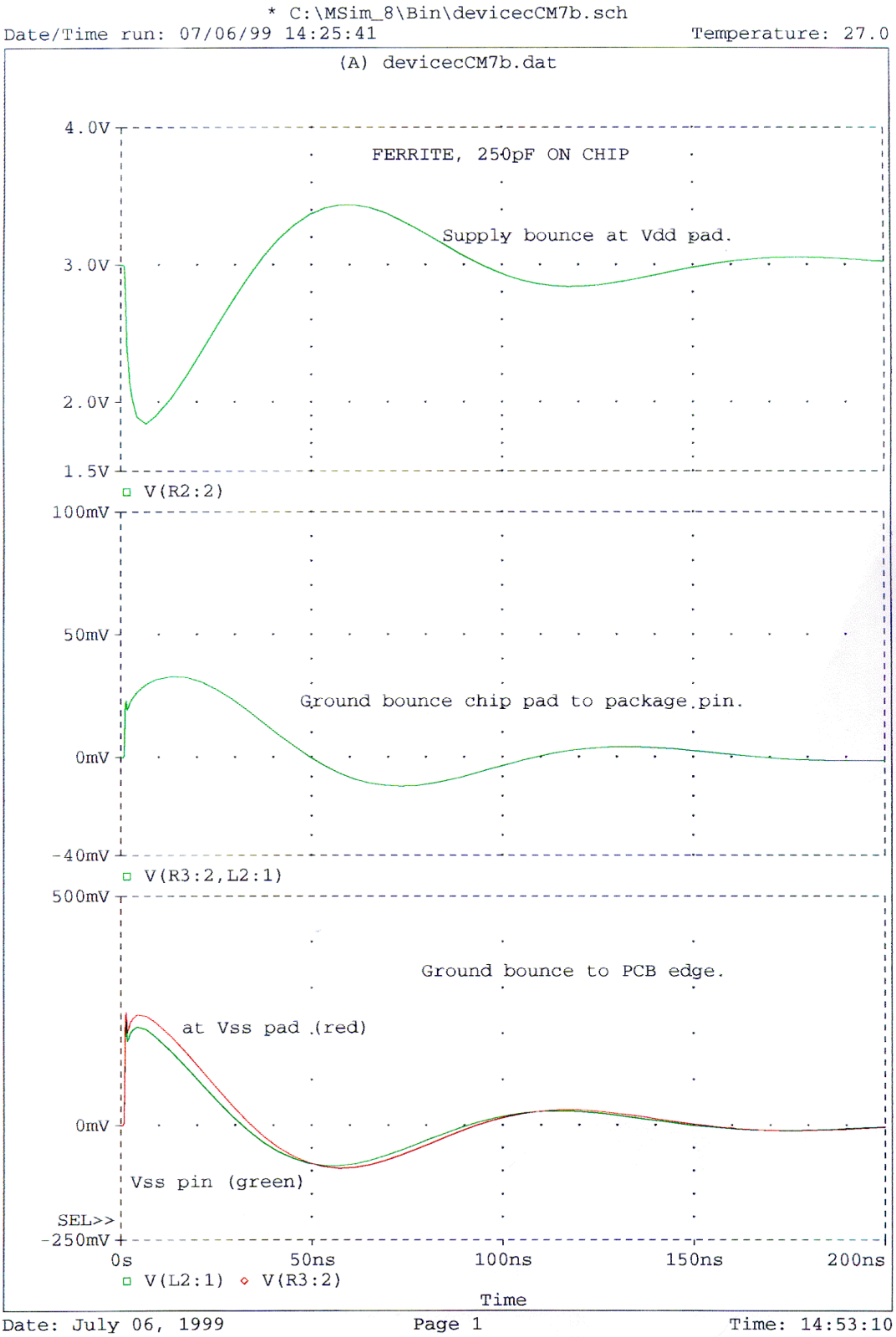


Figure 2.

Here we have the addition of a ferrite bead in the supply line which blocks RF currents, reduces Q and bounce distribution.

Plot 2 (over).

Ground bounce reduces to 200mV (Plot 2a) but note increase in supply bounce! (Plot 2c).



Plot 2a (top), Plot 2b (middle), Plot 2c (bottom).

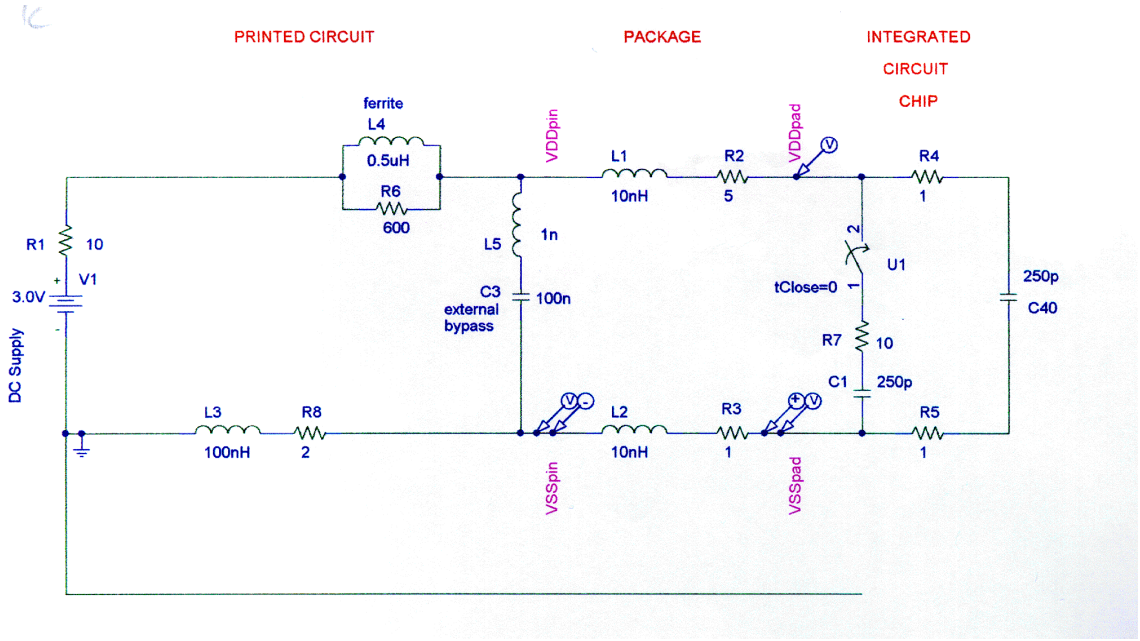
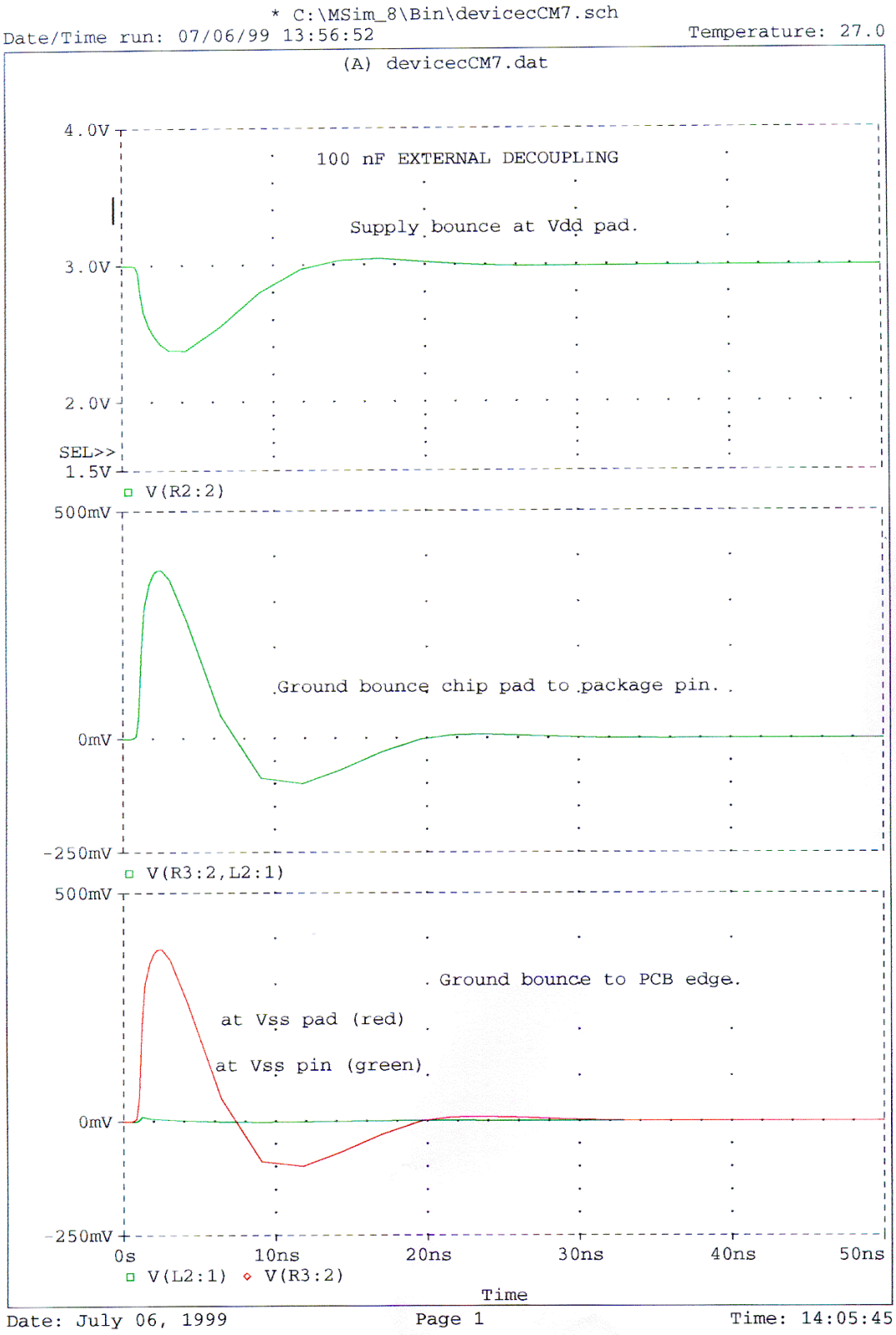


Figure 3.

Here we have the addition of a local external decoupling capacitance to supply charge with the aim of minimising loop area.

Plot 3 (over).

Note that the current flowing across the package inductance, produces a higher ground bounce with this arrangement. (Plot 3c).



Plot 3a (top), Plot 3b (middle), Plot 3c (bottom).

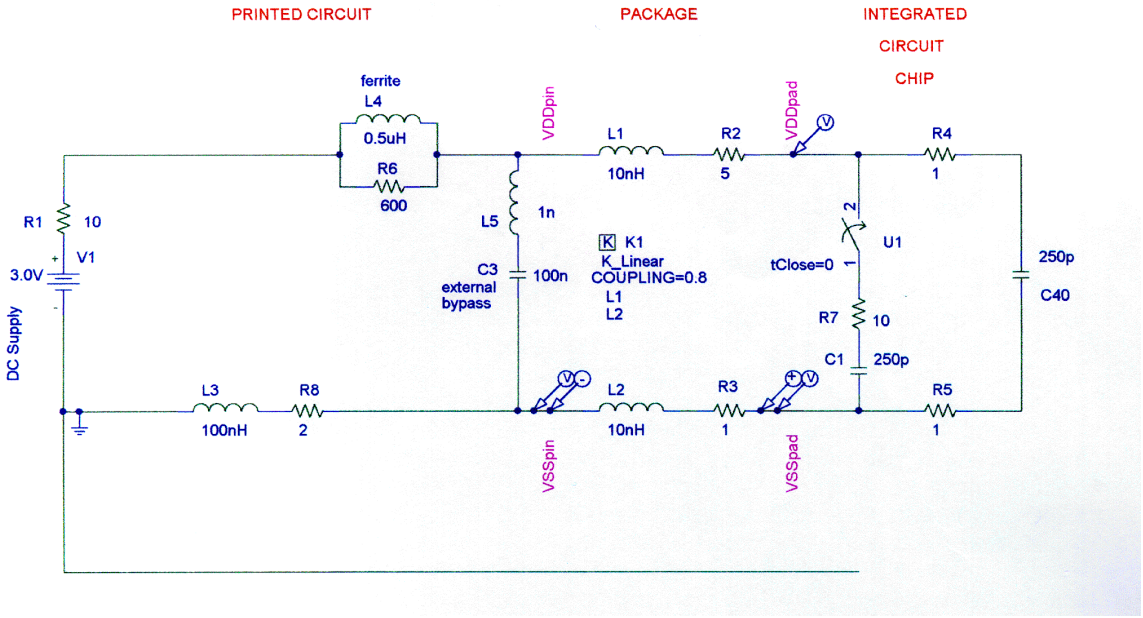
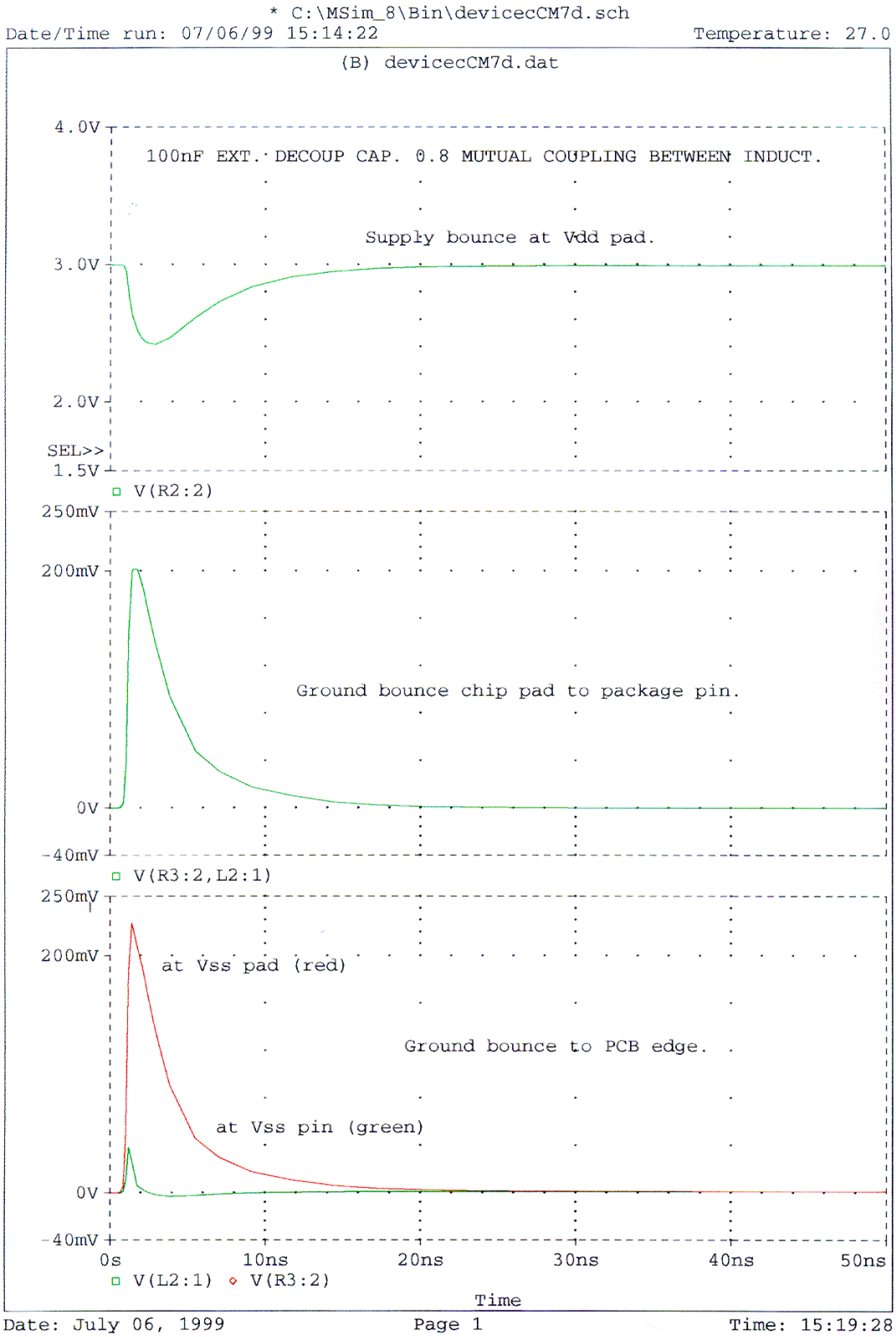


Figure 4.

Supply and ground pins and bondwires can be placed together so that mutual coupling will reduce inductance. A mutual coupling of 0.8 is applied here. (A maximum linear mutual coupling of 1.0 is theoretically, but not practically possible as conductors cannot be co-positioned)

Plot 4 (over).

Ground bounce is halved (Plot 4c) by this simple procedure.



Plot 4a (top), Plot 4b (middle), Plot 4c (bottom).

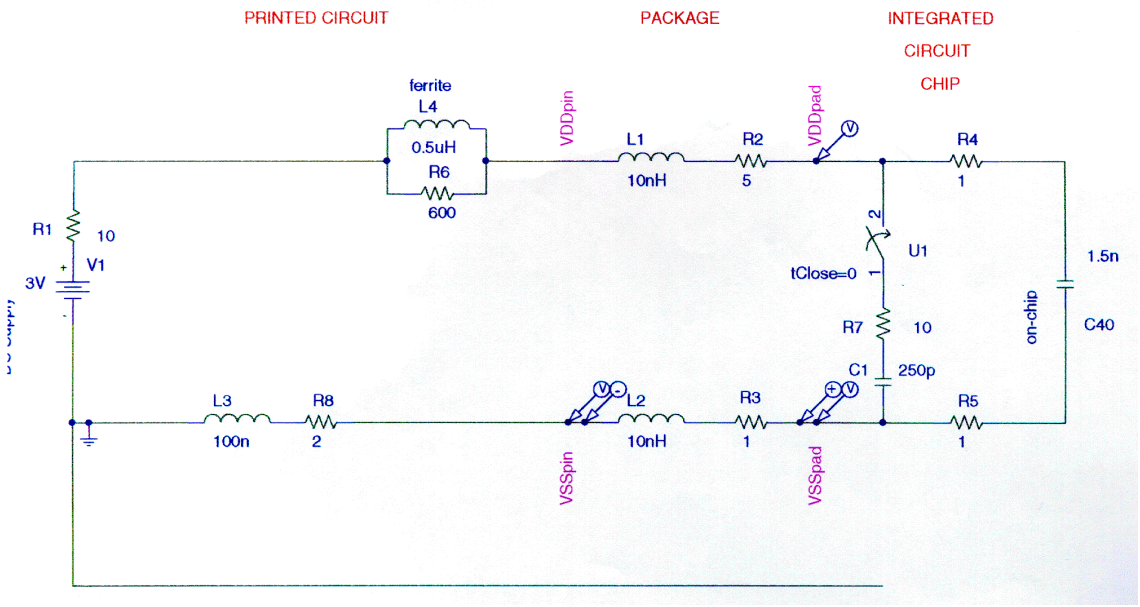
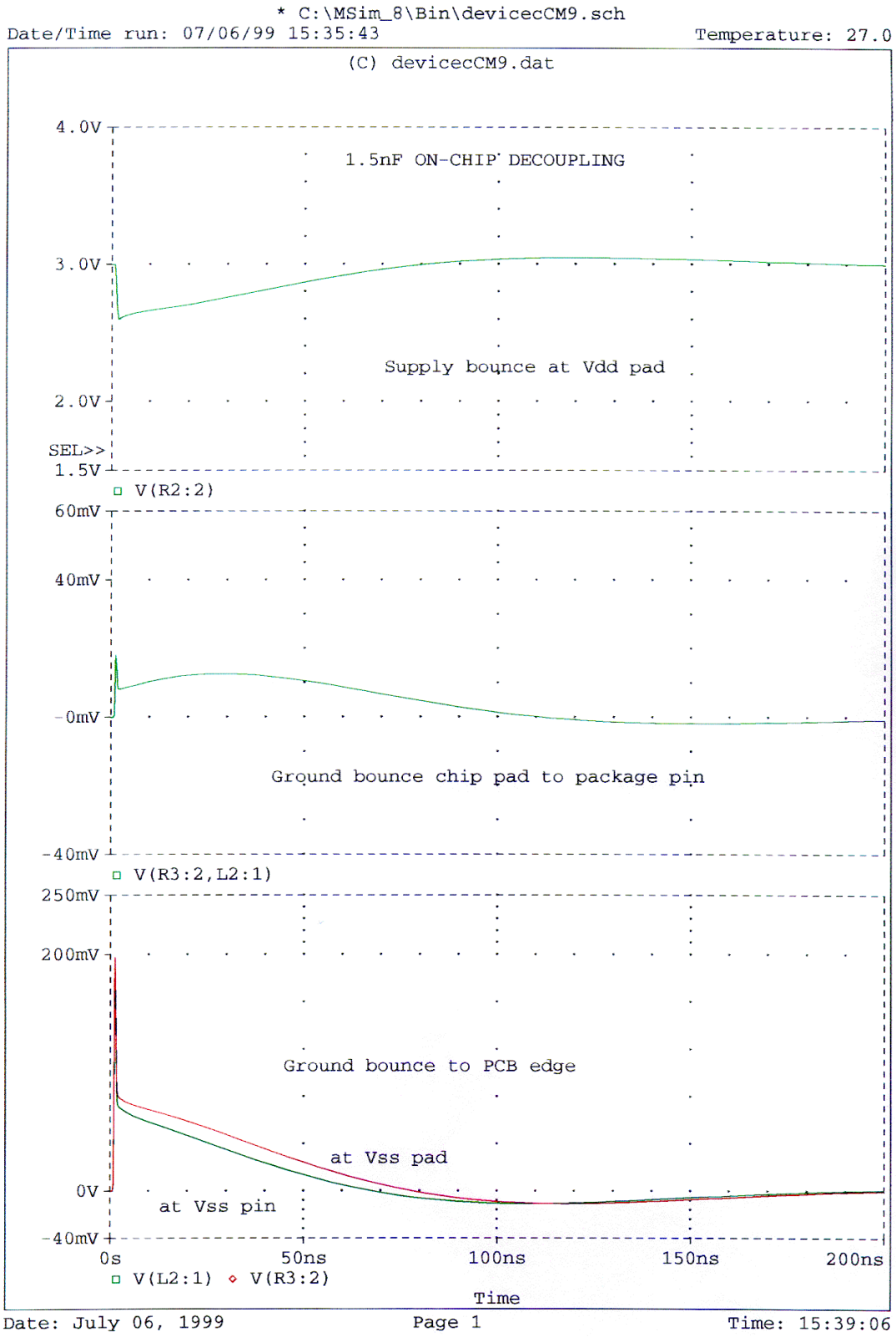


Figure 5.

The external bypassing and mutual coupling has been removed.

Evidently enough on-chip decoupling/bypassing capacitance has been added (as C40), because ground bounce is minimised. See Plot 5 (over).



Plot 5a (top), Plot 5b (middle), Plot 5c (bottom).

Roy Ediss 11-10-2001